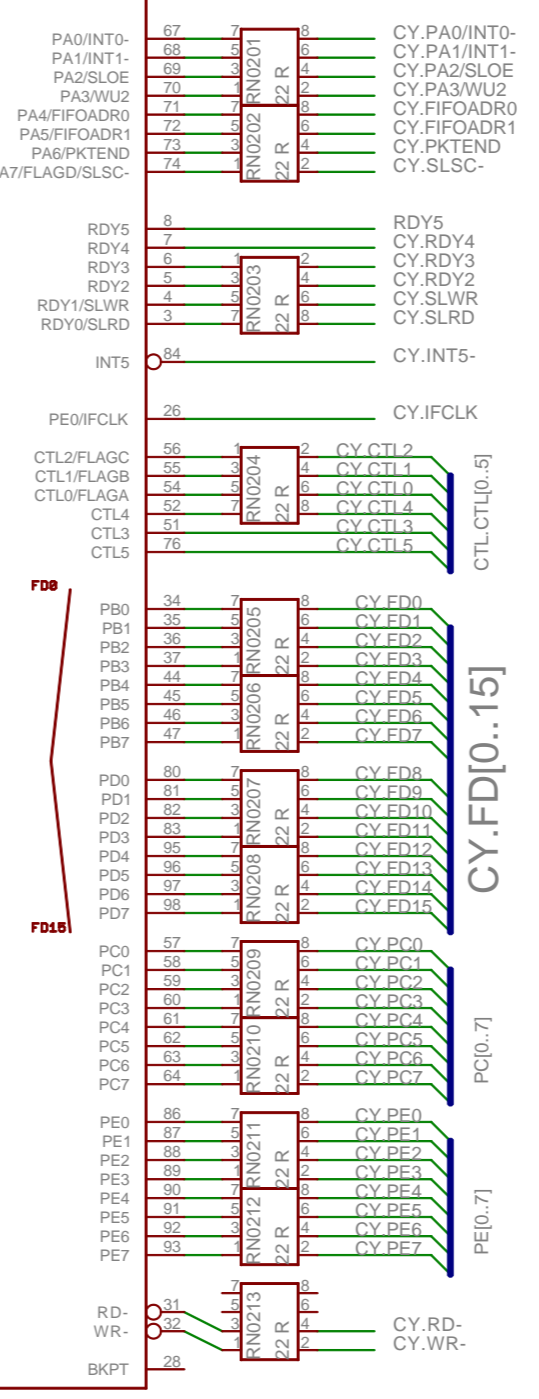
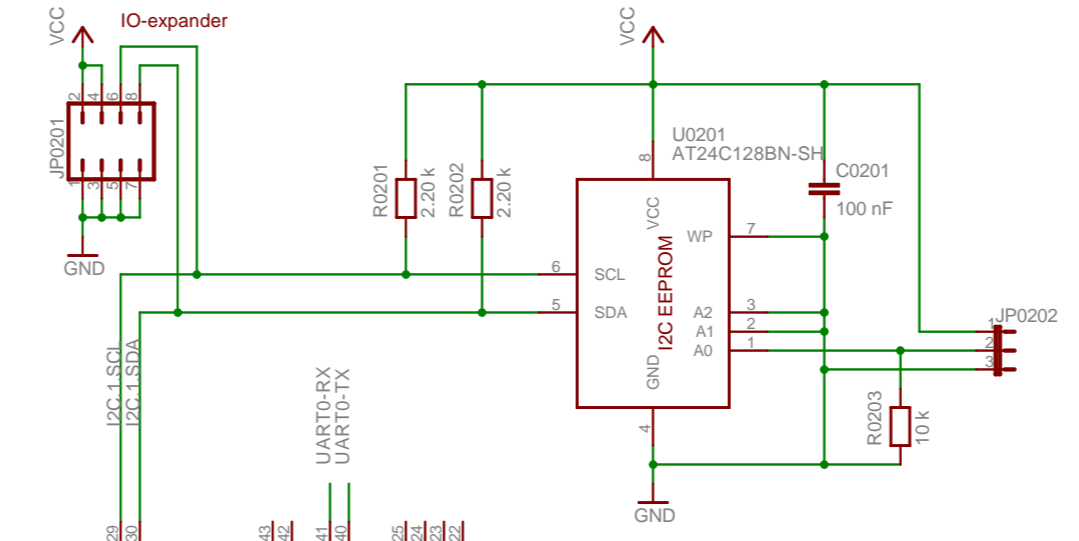
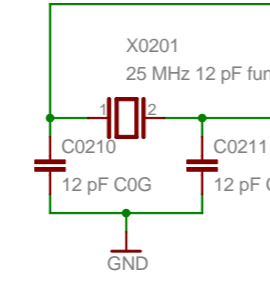
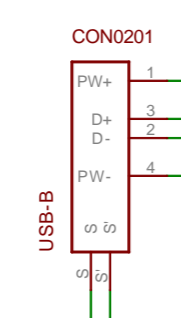
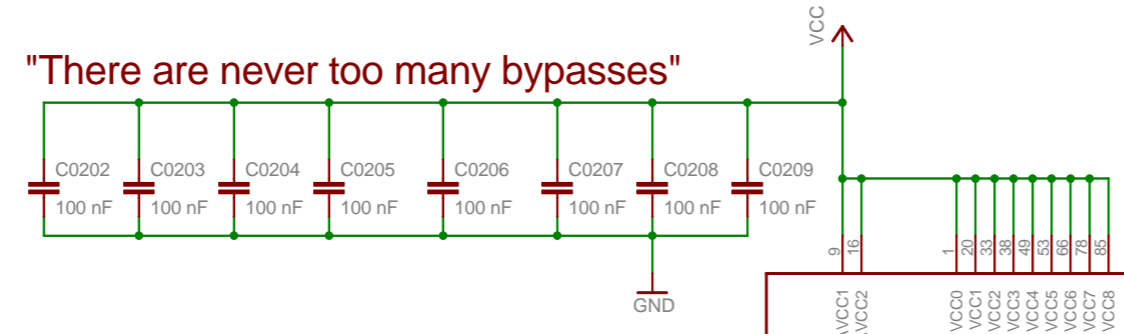


SDR RX USB (High speed)

- 1) Front page
- 2) USB interface
- 3) FPGA glue
- 4) PWR + misc stuff
- 5) AD9874 receiver
- 6) RF frontends
- 7) Master reference oscillator

SDR RX USB (High speed)

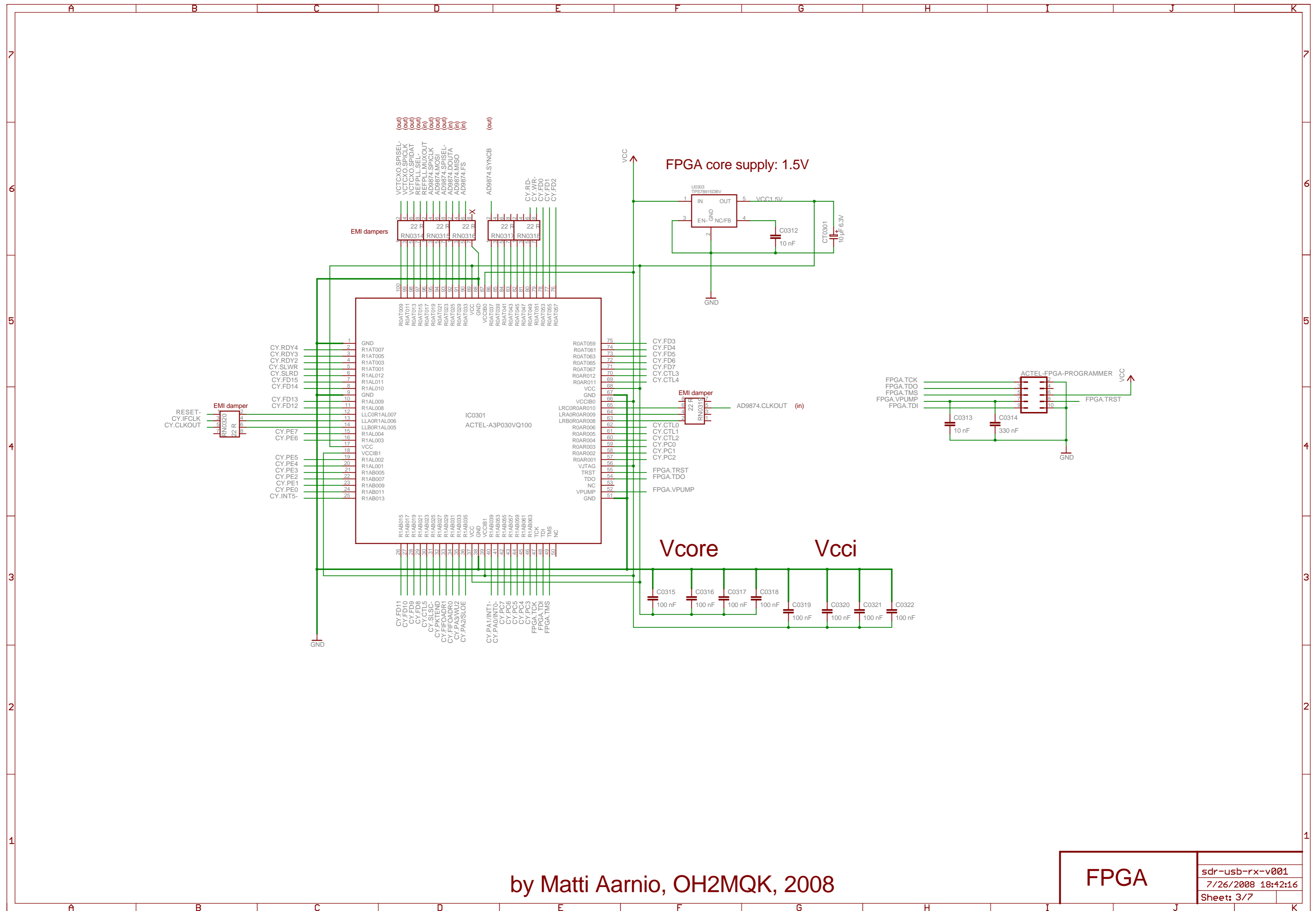
"There are never too many bypasses"



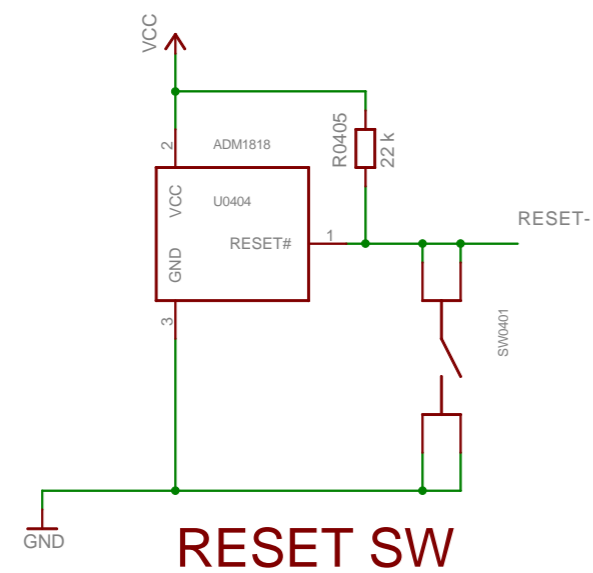
EMI dampers

SDR RX USB (High speed)

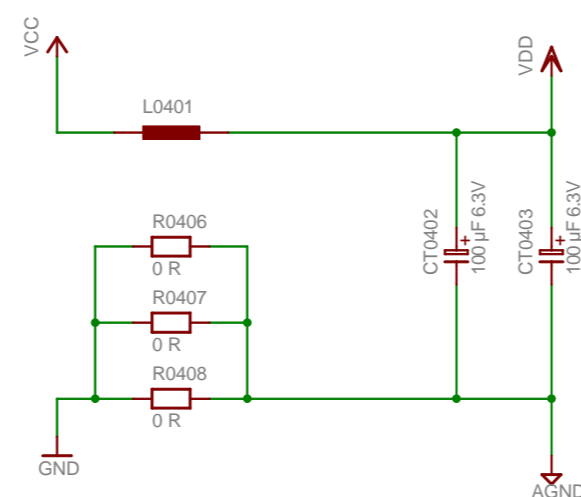
USB IF	sdr-usb-rx-v001
	7/26/2008 18:42:16
	Sheet: 2/7



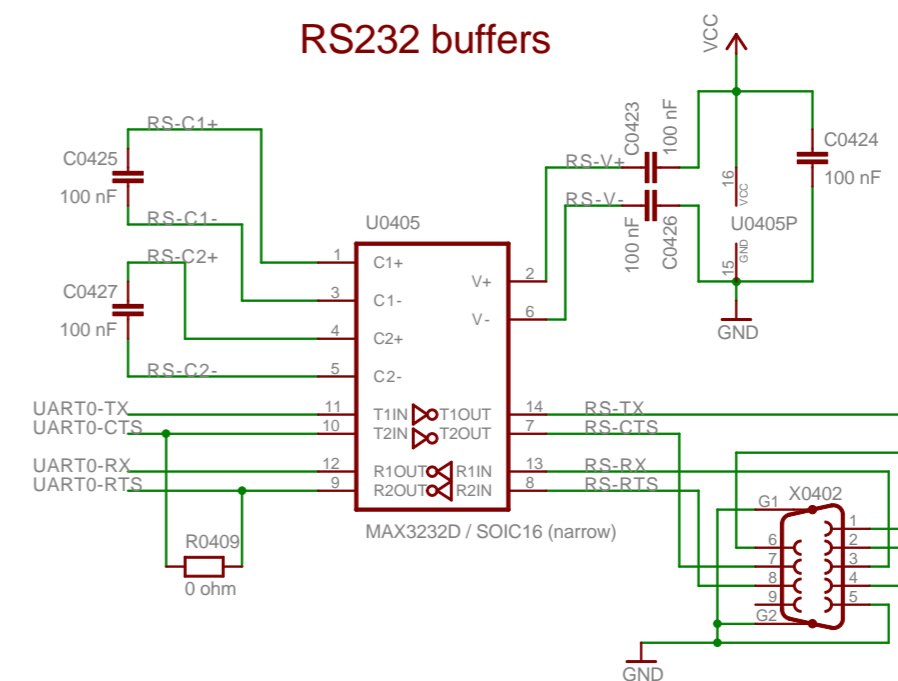
by Matti Aarnio, OH2MQK, 2008



Digital / Analog power plane interconnect



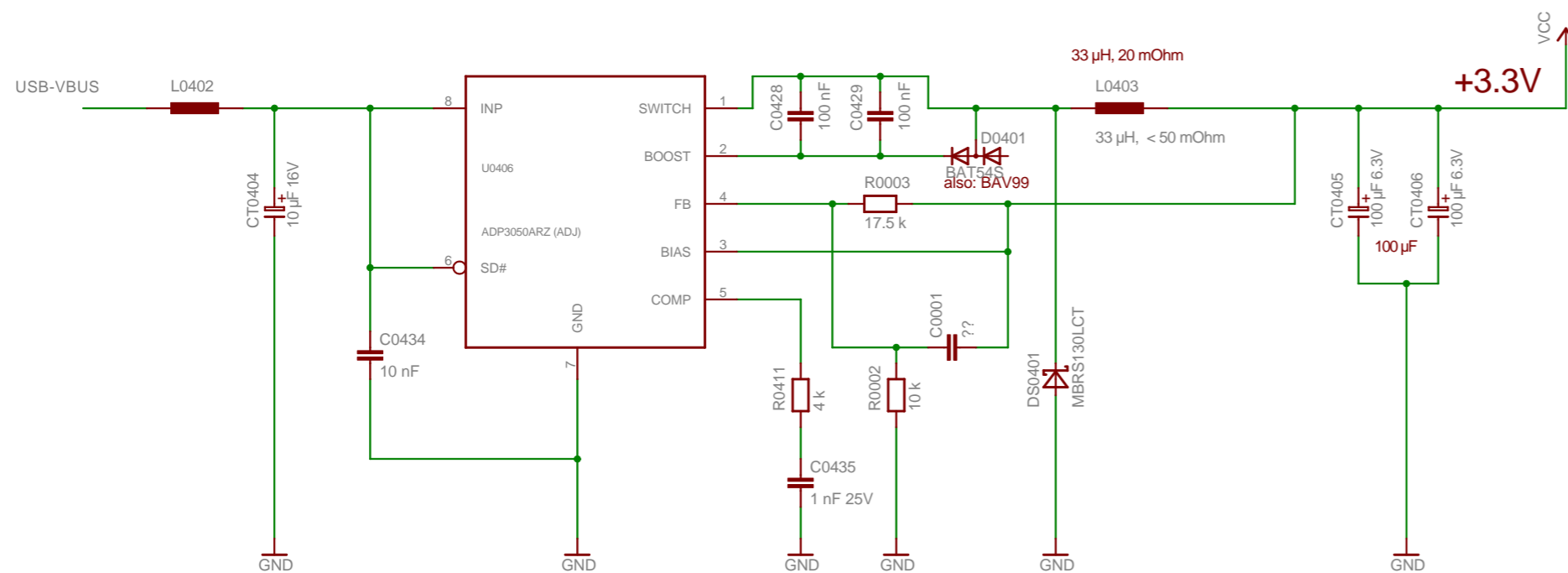
RS232 buffers



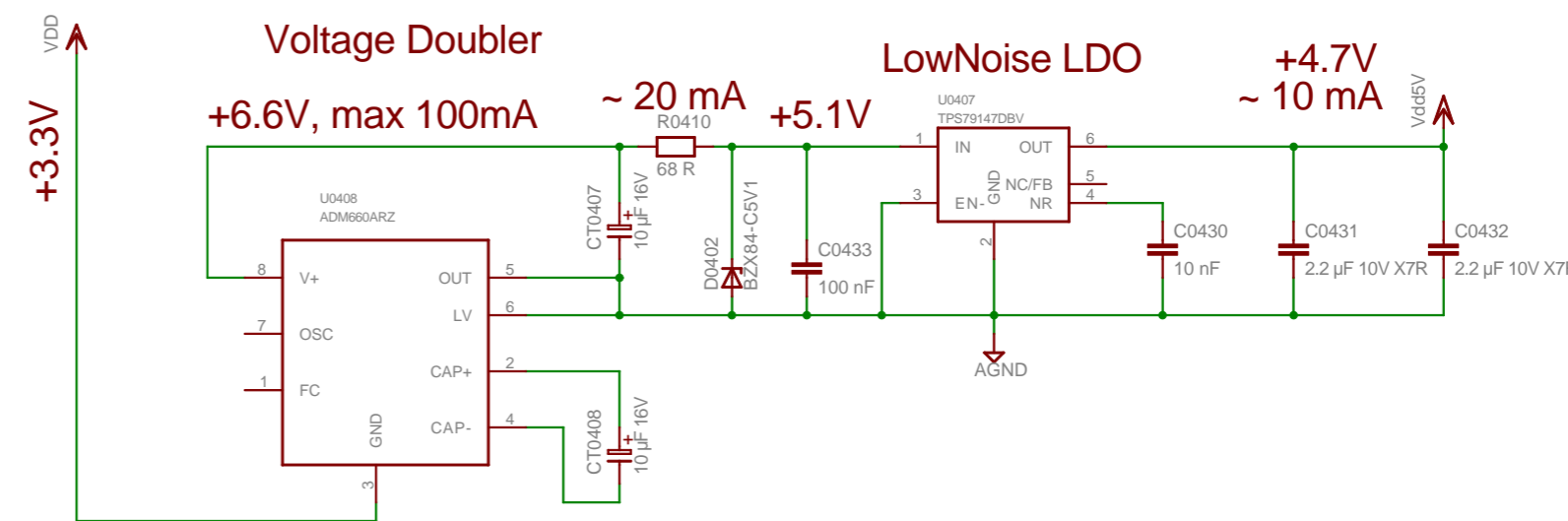
Main SW regulator

input: 4.5 - 15 V

FIXME: verify values



AD9874 CLK & LO SYNTH OPTION PLL SUPPLY



PWR+MISC

sdr-usb-rx-v001
7/26/2008 18:42:16
Sheet: 4/7

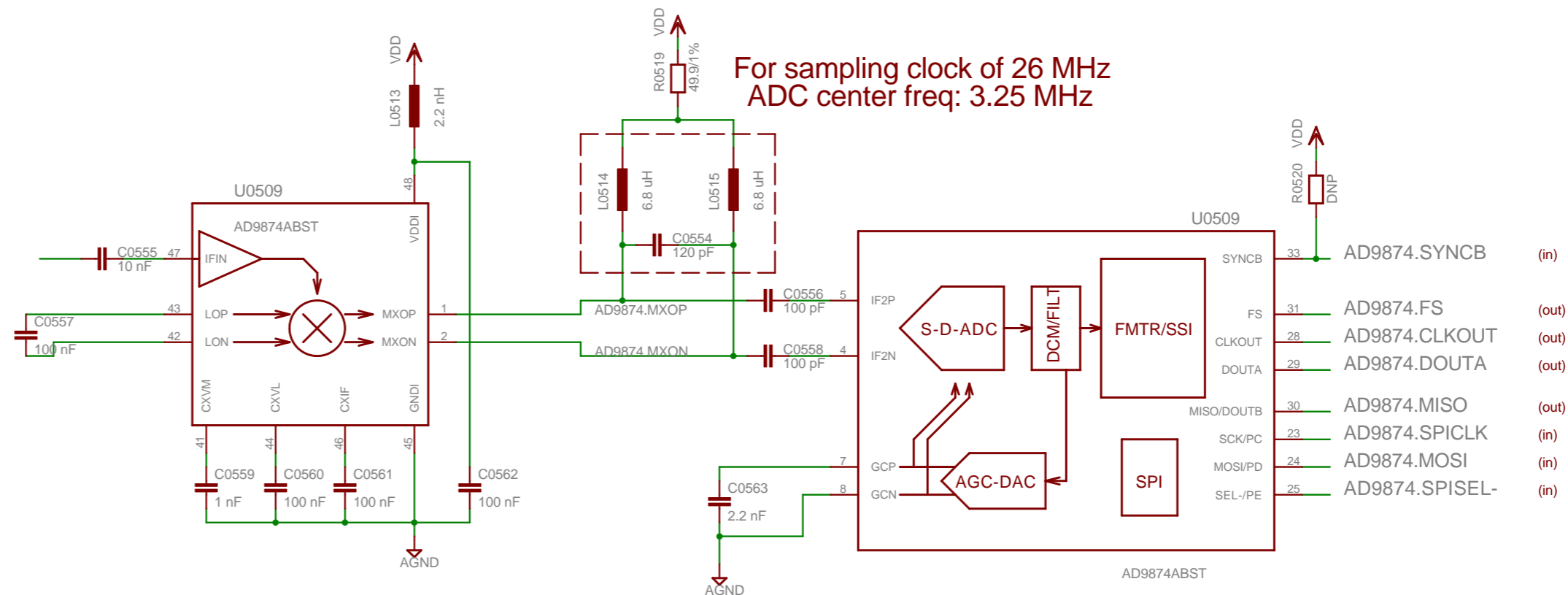
7 TODO: RF input / prefilters

TODO: IF LO

IF = 10.7 MHz

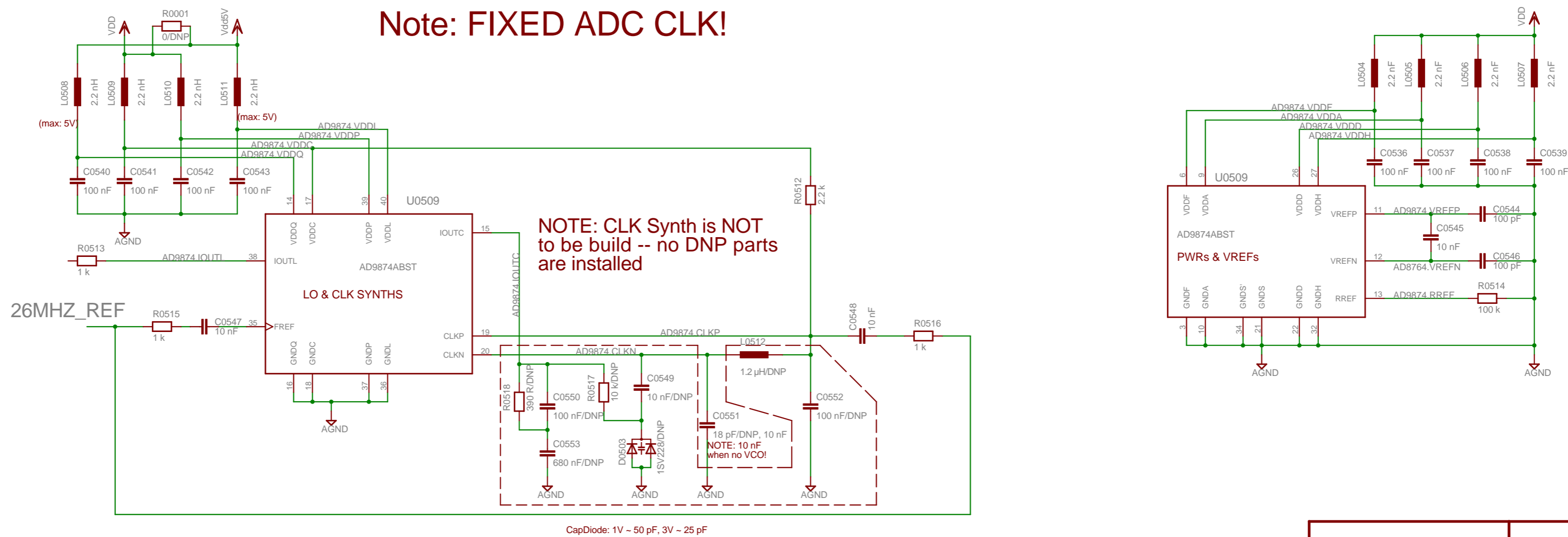
LO = 10.7 - 3.25 / 10.7 + 3.25 MHz

LO = 7.45 / 13.95 MHz



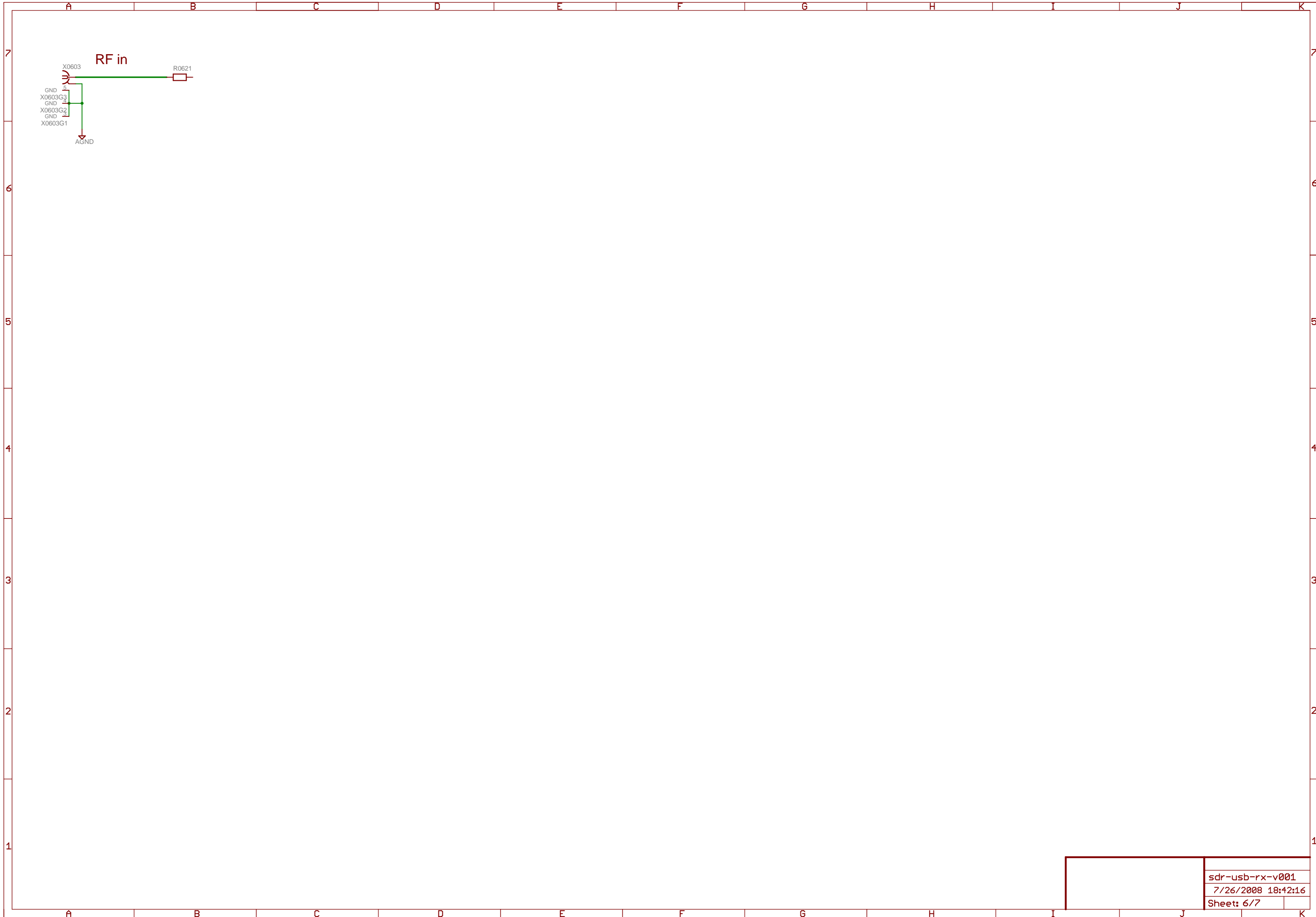
For sampling clock of 26 MHz
ADC center freq: 3.25 MHz

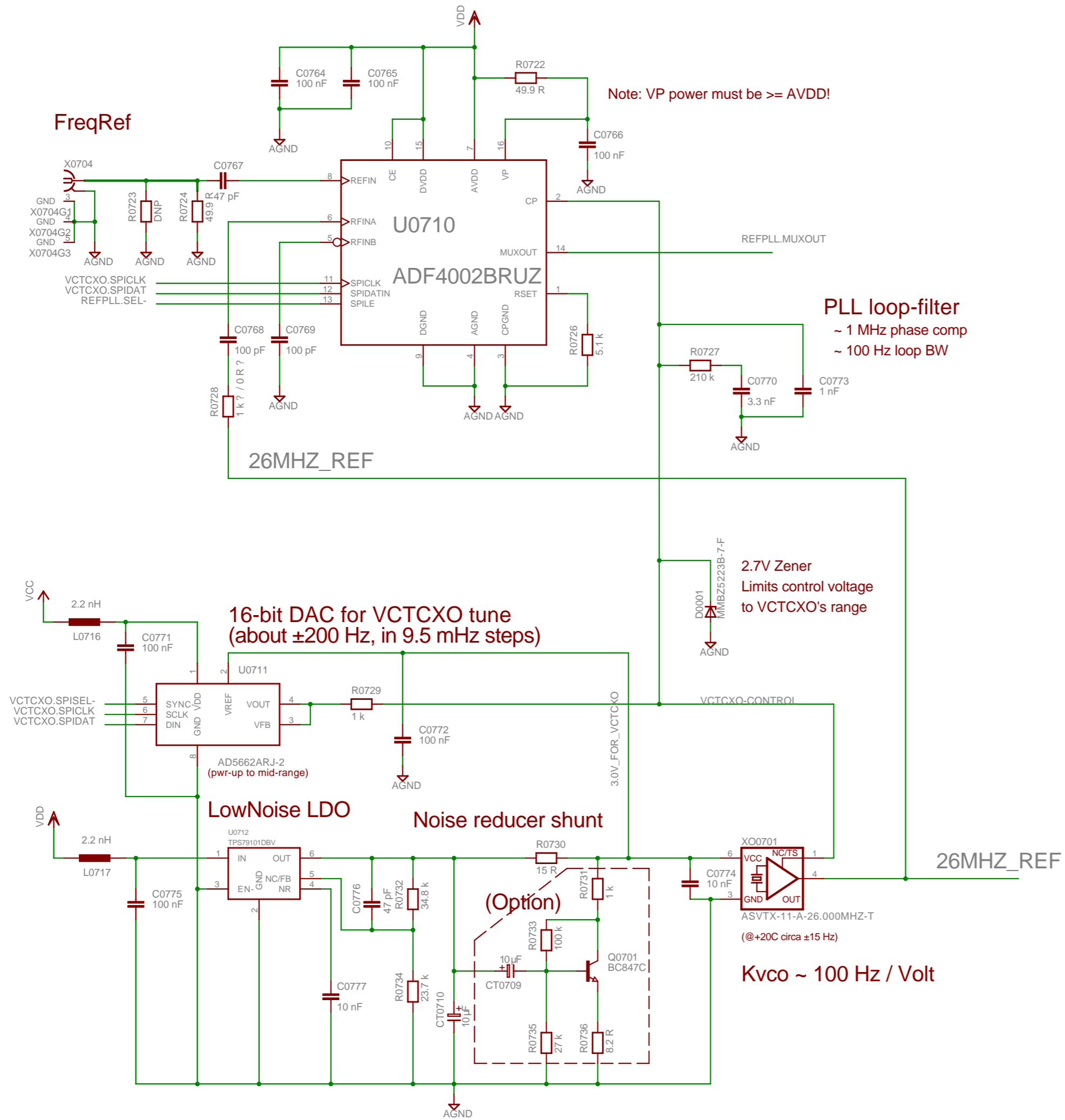
Note: FIXED ADC CLK!



NOTE: CLK Synth is NOT to be build -- no DNP parts are installed

CapDiode: 1V - 50 pF, 3V - 25 pF





At powerup: DAC to mid-range voltage
 .. and ADF400X disabled (CP = HighZ)
 Controller/host initializes the MUXOUT
 to route RefClock to FPGA, where mode
 is to act as frequency counter.
 If counter yields some multiple of 1 MHz
 controller/host sets dividers to GCD of that
 frequency, and 26 MHz, disables DAC and
 enables PLL. The MUXOUT reports lock.
 Essentially this can lock on ANY reference
 of exact MHz in between 1.0 and 150 MHz,
 also perhaps at 2.5 MHz.
 FPGA freq-counter is upper limit for the Fref.