

# SDR DSP base board

version 1 proto

Page:

- 2 Analog Devices Blackfin DSP: BF531/2/3
- 3 SDRAM 16/32/64/128 MB  
Flash memory: 2/4/8 MB
- 4 Glue logic CPLD
- 5 Power supply
- 6 SPORT connectors, CFLASH socket
- 7 USB interface
- 8 Board dimensions

Note: component numbering runs as: <prefix><sheet\_number><sequence\_number>  
where <sheet\_number> is always 2 decimal digits, while <sequence\_number> has at least two digits.

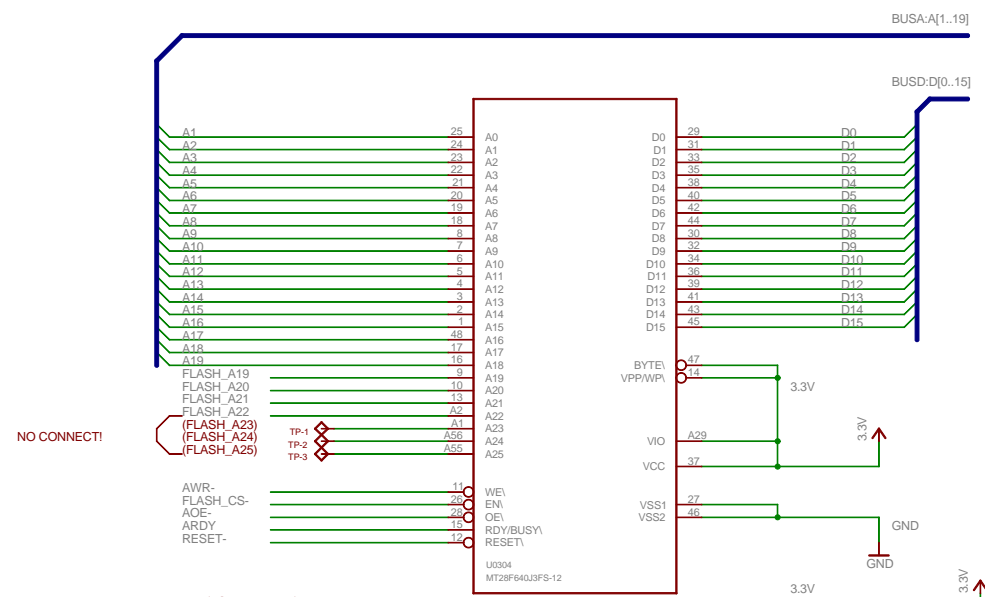
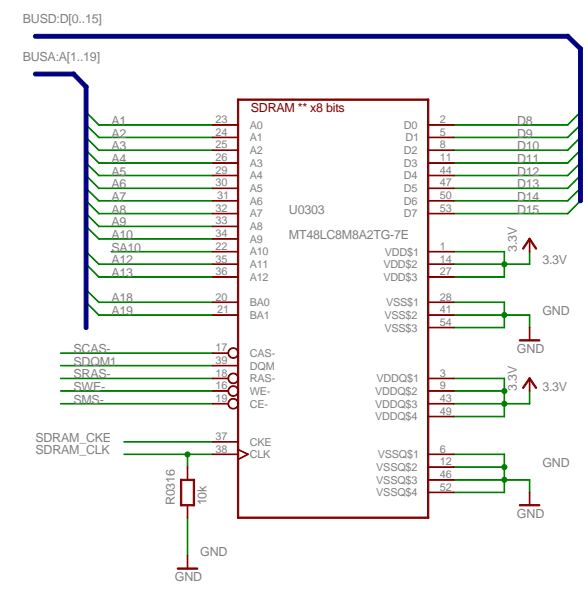
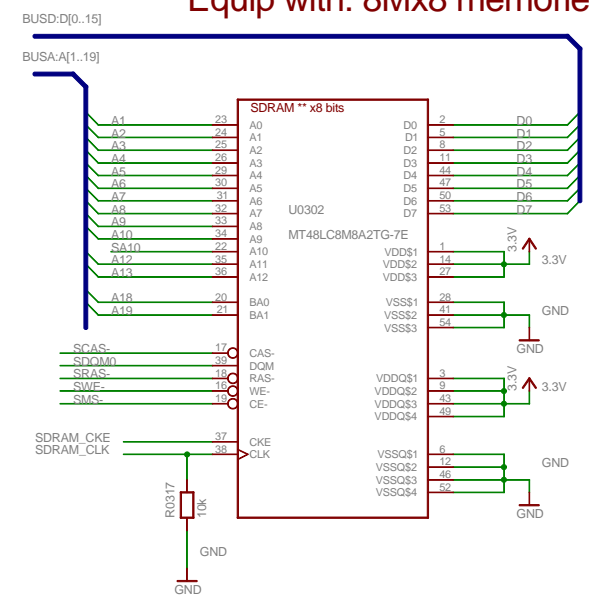
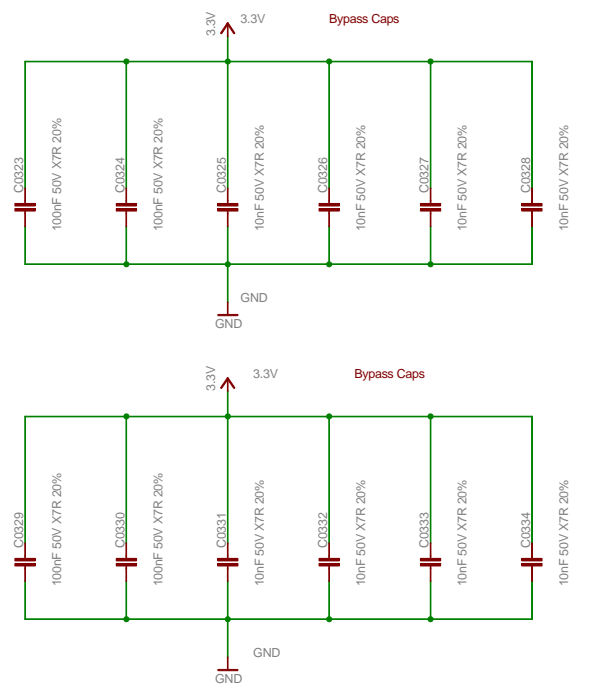
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8/10/2005 12:03:40
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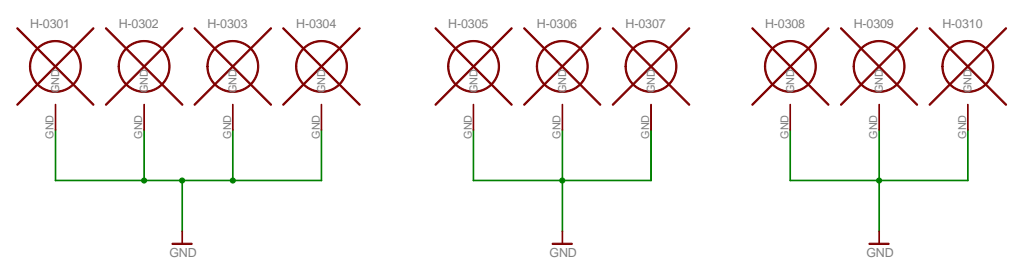
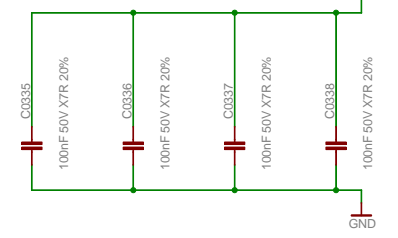


**MAX SDRAM: 128 MB !**  
**Equip with: 8Mx8 memories, total 16 MB**



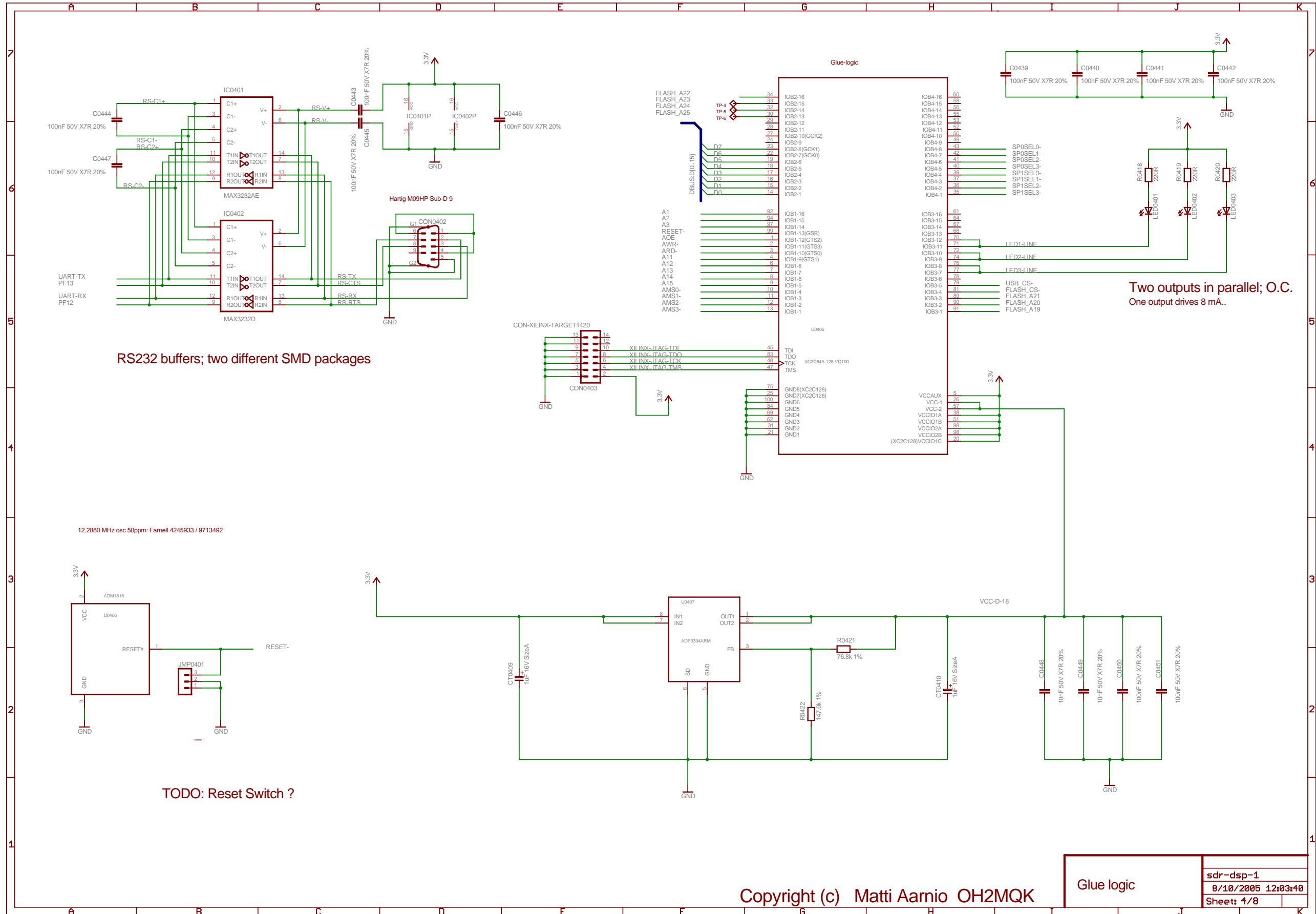
Low 1st megabyte (ASM0- selected) is direct mapped  
 ASM1- selected memory area refers to arbitrary memory block

**Equip with 8MB flash**



SDRAM max 128 MB	sdr-dsp-1
FLASH max 16 MB	8/10/2005 12:03:40
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RS232 buffers; two different SMD packages

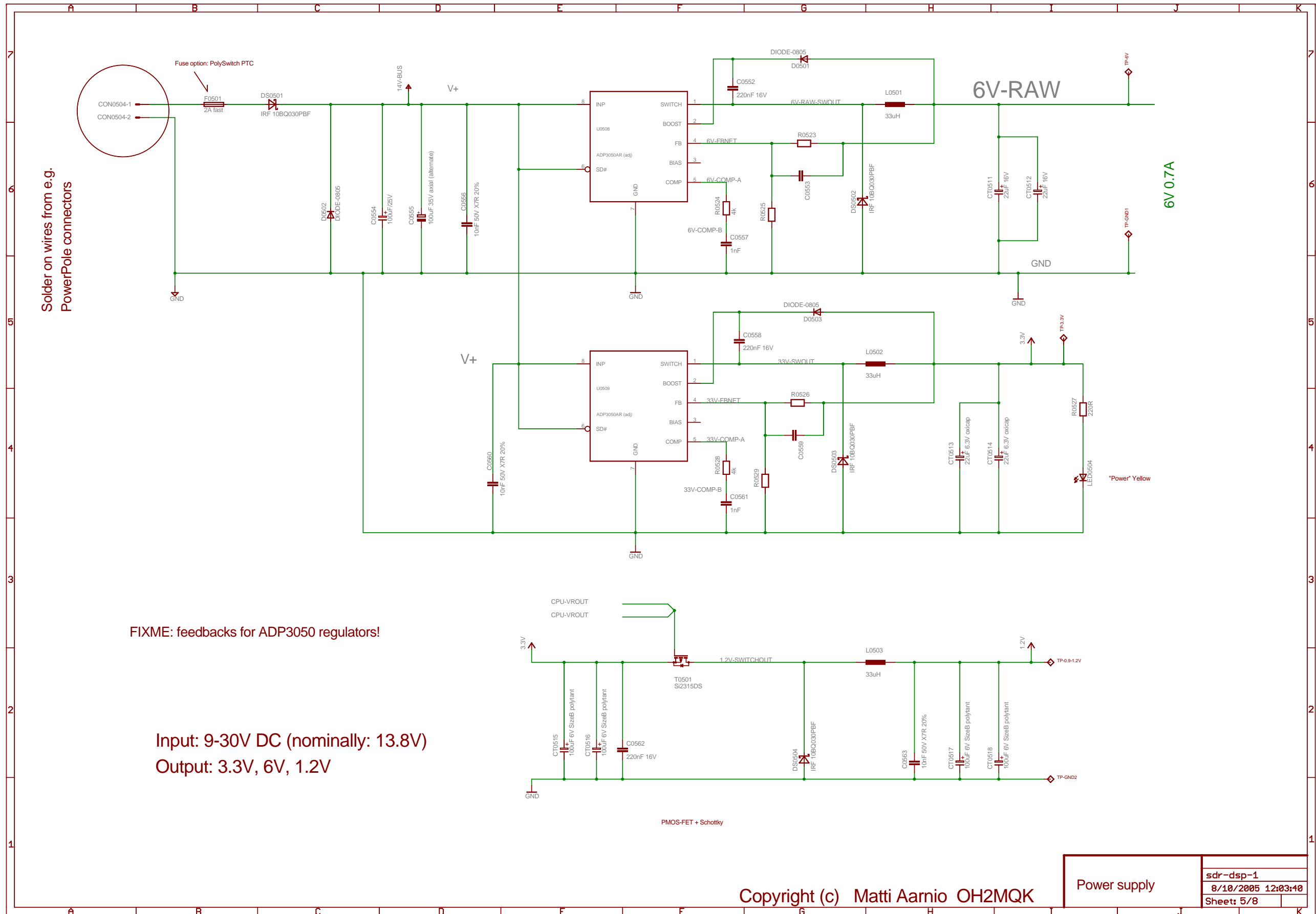
Two outputs in parallel; O.C.  
One output drives 8 mA.

TODO: Reset Switch ?

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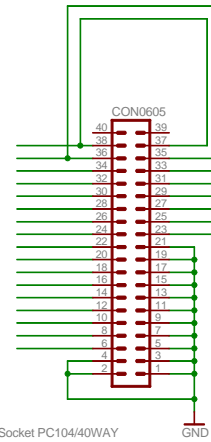
Glue logic

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### SPORT connectors

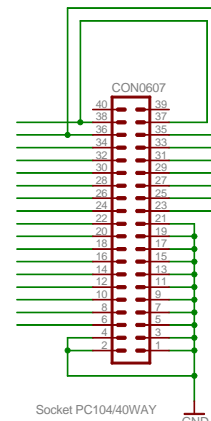
6V-RAW  
3.3V  
PF4  
PF2  
RESET-  
SPL\_CLK  
SPL\_MISO  
SP0SEL2-  
SP0SEL0-  
DT0SEC  
DT0PRI  
TFS0  
TSCLK0  
DR0SEC  
DR0PRI  
RFS0  
RSCLK0



For LDO regulation at IF board  
PF5  
PF3  
PF1  
SPL\_MOSI  
SPOSEL3-  
SPOSEL1-

Socket PC104/40WAY

6V-RAW  
3.3V  
PF9  
PF8  
RESET-  
SPL\_CLK  
SPL\_MISO  
SP1SEL2-  
SP1SEL0-  
DT1SEC  
DT1PRI  
TFS1  
TSCLK1  
DR1SEC  
DR1PRI  
RFS1  
RSCLK1

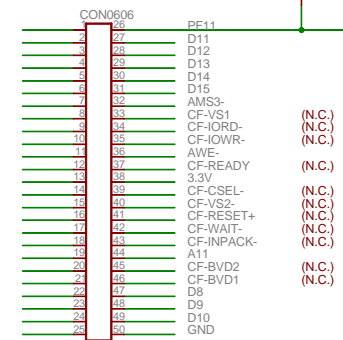


For LDO regulation at IF board  
PF10  
PF7  
PF6  
SPL\_MOSI  
SP1SEL3-  
SP1SEL1-

Socket PC104/40WAY

### Compact Flash socket

GND  
D3  
D4  
D5  
D6  
D7  
AMS3-  
A10  
AOE-  
A9  
A8  
A7  
3.3V  
A6  
A5  
A4  
A3  
A2  
A1  
GND  
D0  
D1  
D2  
(N.C.)  
(N.C.)  
CF-WP  
CF-CD2-

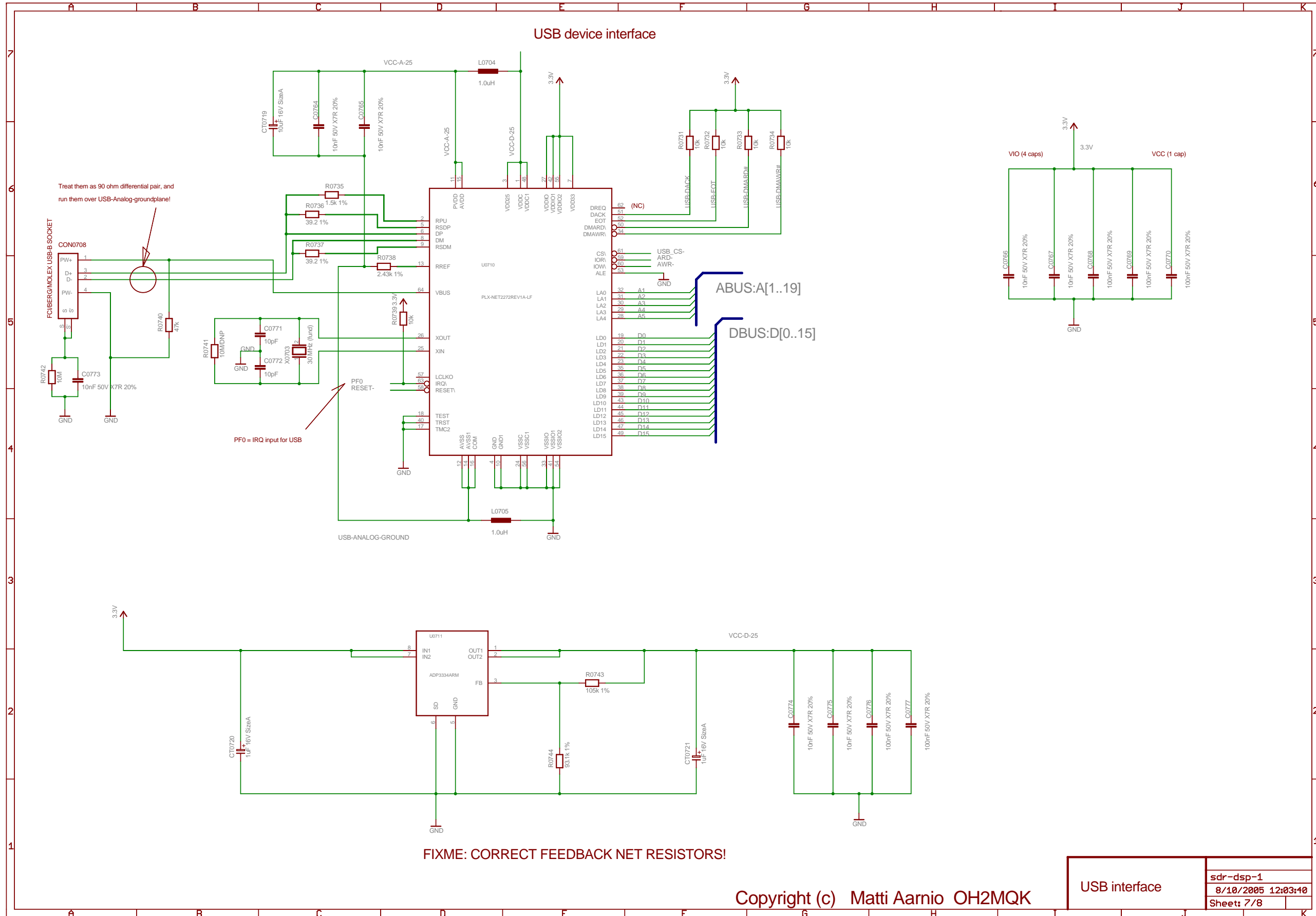


3.3V  
R00B30  
10k

3M N7E50-7516-VY (+ 3503-34 ?)

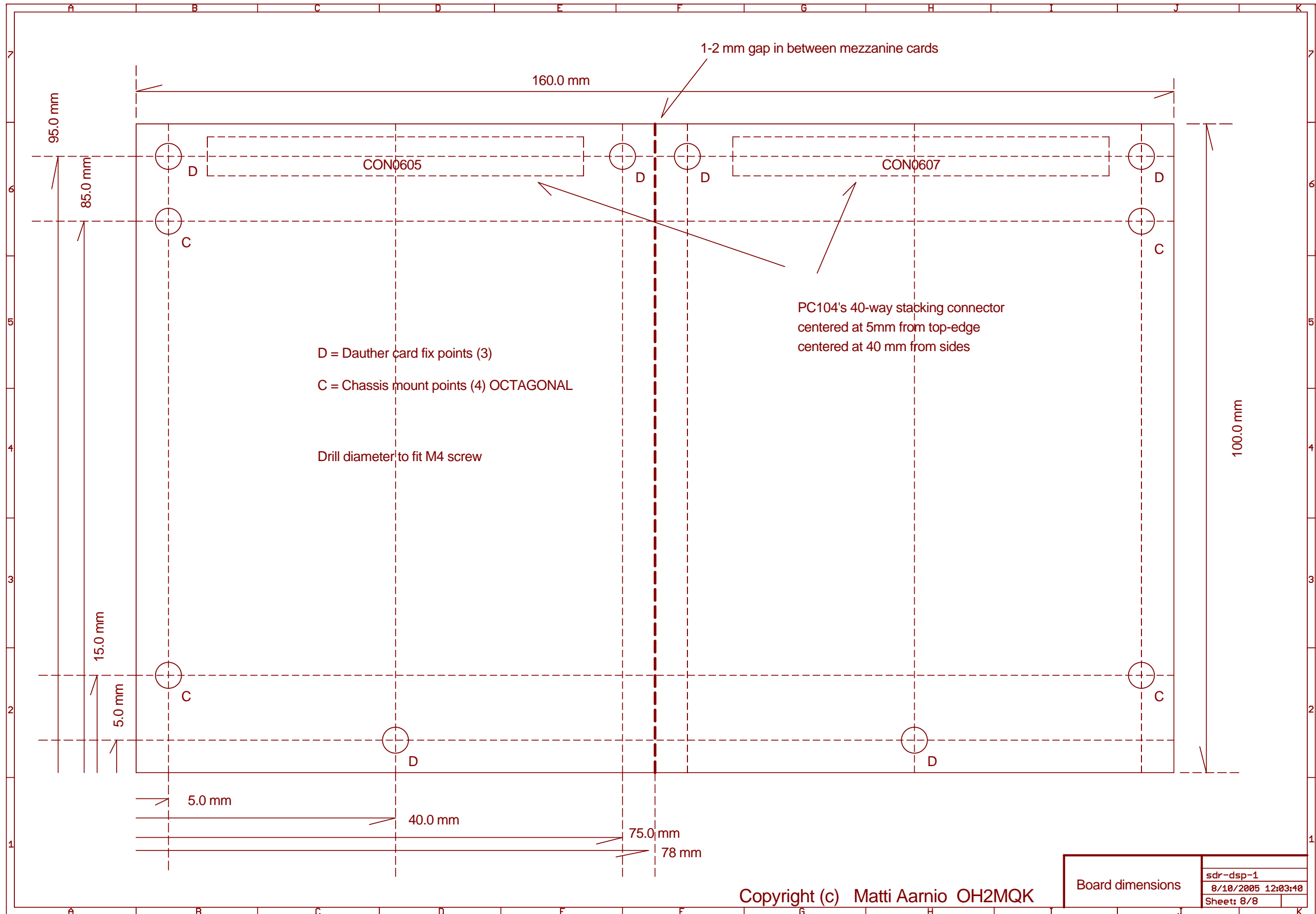
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SPORT connectors	sdr-dsp-1
CFLASH socket	8/10/2005 12:03:10
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USB interface	sdr-dsp-1
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